

**AMENDMENTS TO THE SPECIFICATION:**

Please replace the paragraph beginning on page 4, line 6 and ending on page 4, line 12, with the following amended paragraph:

The operation of the conventional clock data recovery circuit is explained next. The phase comparator 100 compares the phase of the input data DIN with the phase of ~~the clock 4~~ the clock CLK 1 generated by the VCO 300, and detects a phase difference between these two signals, as described above. The phase comparator 100 outputs the detected phase difference as the analog phase difference signal FEO1, to the LPF 200.

Please replace the paragraph beginning on page 26, line 6 and ending on page 26, line 13, with the following amended paragraph:

The phase comparator 81 compares a phase of the frequency-divided input data RZ-DATAR with a phase of a clock CLKR generated by the VCO 83, and detects a phase difference between these two signals. The phase comparator 81 outputs a phase difference signal FEOR, which shows the detected phase difference in an analog value, to the LPF 82. The configuration of the phase comparator ~~[[91]]~~ 81 is the same as that of the phase comparator 1 according to the first embodiment shown in Fig. 2, and its explanation is omitted.

Please replace the paragraph beginning on page 26, line 21 and ending on page 26, line 23, with the following amended paragraph:

The second clock generating circuit 9 generates a clock ~~[[CLKR]]~~ CLKF of which phase coincides with a phase of a falling edge of the input data RZ-DATA.

Please replace the paragraph beginning on page 27, line 11 and ending on page 27, line 17, with the following amended paragraph:

The LPF 92 smoothes the phase difference signal ~~[[FEOR]]~~ FEOF by removing a higher frequency component from this signal, thereby obtaining a voltage control signal, and outputs this voltage control signal to the VCO 93. The VCO 93 generates the clock CLKF by adjusting the oscillation frequency based on the voltage control signal, and outputs the generated clock ~~[[CLKR]]~~ CLKF to both the phase comparator 91 and the phase combiner 10.

Please replace the paragraph beginning on page 28, line 20, and ending on page 29, line 4, with the following amended paragraph:

As shown in Fig. 12, the frequency divider 85 of the first clock generating circuit 8 detects the rise of the input data RZ-DATA, and inverts the output frequency-divided input data RZ-DATAR. The frequency divider 95 of the second clock generating circuit 9 detects the fall of the input data RZ-DATA, and inverts the output frequency-divided input data RZ-DATAF. In other words, the frequency-divided input data RZ-DATAF output from the second clock generating circuit 9 is delayed from the frequency-divided input data RZ-DATAR output from the first clock generating circuit ~~[[9]]~~ 8 by the bit width of the input data RZ-DATA.